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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	Mostafazadeh, Shahram; Smith, Joseph O.		
Assignee:	National Semiconductor Corporation		
Title:	LEAD FRAME DESIGN FOR INCREASED CHIP PINOUT		
Serial No.:	09/054,380	Filed:	April 2, 1998
Batch No.:	C12	Date Allowed:	September 27, 1999
Examiner:	H. Duong	Group Art Unit:	2823
Docket No.:	NS-3856 US		

San Jose, California

BOX ISSUE FEES
Attn: Official Draftsperson
ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

SUBMISSION OF FORMAL DRAWINGS

Dear Sir:

Applicants submit four (4) sheets of formal drawings, consisting of Figures 1a-1, 1a-2, 1b-1, 1b-2, 1c-1, 1c-2, 2a-1, 2a-2, 2b-1, 2b-2, 2c-1, 2c-2, 2d-1 and 2d-2, in the above-named application. If there are any questions regarding these drawings, please call the undersigned at (408) 453-9200.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on November 10, 1999.

Attorney for Applicant(s) — Date of Signature: 11/10/99

Respectfully submitted,

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